Gate Insulators in Organic Field-Effect Transistors

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In this paper, we review recent progress in the understanding of insulator/semiconductor interfaces in organic field-effect transistors (OFETs). We would like to emphasize that the choice of gate insulator is as important for high-quality OFET devices as the semiconductor itself, especially because of the unique transport mechanisms operating in them. To date researchers have explored numerous organic and inorganic insulator materials, some of them designed to improve the morphology of the organic semiconductor (OSC). Surface treatments, particularly on inorganic insulators, have been shown to influence significantly molecular ordering and device performance. In addition, the deposition technique used for the insulator and semiconductor layers has a further impact on the active interface. Dielectric related effects are reviewed here for a variety of polymeric and molecular semiconductors reported in the literature, with an emphasis on electronic transport. We also review in more detail experiences at Philips and the recent work at Avecia to clarify some of the interface phenomena using amorphous OSC.

Introduction

The use of organic materials to build electronics is most attractive for low cost devices fabricated by printing techniques on large area, flexible substrates. The idea of organic materials behaving as semiconductors is almost as old as inorganic electronics.[1] High-quality transistor devices, however, had to wait until the past decade when high purity organic materials (Figure 1) were employed and deposition techniques were refined. Early organic electronics was really a hybrid: inorganic materials such as thermally grown SiO_2 gate insulators were combined with organic semiconductors. SiO_2 was most convenient, as it was readily available from conventional Si technology. SiO_2 is still widely used in benchmark test devices. In the past years, intensive effort has been spent on what is perceived to be the most difficult task: developing new polymeric or molecular semiconductors with mobilities approaching that of amorphous silicon.[2,3] It has become clear that such high mobilities, being on the edge of band transport, require a high degree of molecular alignment. Consequently, deposition techniques were optimized for materials such as pentacene and poly-3-hexylthiophene (P3HT) to maximize ordering and in turn carrier mobility. In these experiments, mostly bottom gate OFETs were used, and consequently, the role of the gate insulator was even more critical, as it also served as the substrate. In some cases prealigned, rubbed substrates were used to enhance molecular orientation. Monomolecular surface treatments were also employed to influence interactions with OSC polymers or molecules. The role of the gate insulator, therefore, has most frequently been treated as the layer affecting semiconductor morphology. However, the dielectric can influence the OSC and OFET operation in many more ways, as will be discussed below. This paper attempts to review the current understanding of the influence of dielectrics in OFETs, but the scope will be limited to electronic transport. The requirements for a practical dielectric in an OFET are much broader and include processability, high capacitance, high dielectric strength, high on/off ratio, low hysteresis, etc.[4] Therefore, these topics could be the topic of a separate paper.

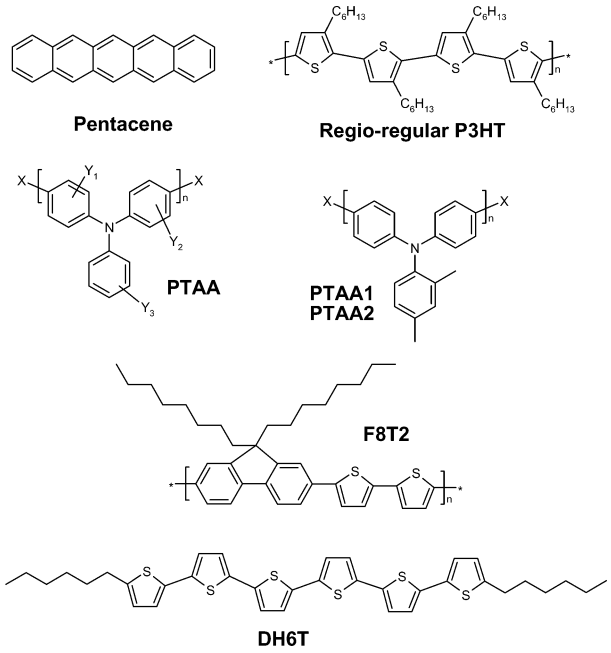

Figure 1. Chemical structures of some organic semiconductors discussed in this review.

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Potential Dielectric Effects in OFET

The conduction mechanism in organic semiconductors is different from that in inorganics. Due to the weak intermolecular forces in OSC, true bands rarely form and carriers move instead by hopping. Only at low temperatures in molecular crystals can one observe band-like transport. Organic semiconductors are basically, "molecular solids", even in the case of polymeric OSC (Figure 1). As a result, the number of effects through which the dielectric can influence carrier transport and mobility is much broader than in inorganic materials. First, and foremost, the dielectric can affect the morphology of OSC and the orientation of molecular segments, via their interaction with the dielectric (especially in bottom gate devices). Second, the interface roughness and sharpness may be influenced by the dielectric itself, the deposition conditions, and the solvents used. Studies of interface roughness indicate that it is a key parameter in OFETs. Increased roughness leads to valleys in the channel region, which may act as carrier traps. Roughness also inhibits the growth of uniform, large crystal domains and affects the nucleation density of polycrystalline materials. Another intriguing effect in OFETs is gate voltage dependent mobility, which, together with the variation of threshold voltages, can be a signature of dielectric interface effects. A further possibility is that the carrier concentration induced across the insulator modulates the mobility itself by changing the occupation level of the interface density of states (DOS). At the same time, the gate field may force the carriers to travel in the vicinity of the interface in a 2D fashion rather than allowing them to optimize their route through more efficient paths through the 3D bulk. Distinguishing between the two has not been an easy task so far. High capacitance is normally desirable, as it allows the reduction of the threshold voltage and operating voltage, while achieving this at lower gate field. Threshold voltages may be due to built-in charge but may also be the indication of interface states (undesirable chemical groups/sites on the insulator itself or foreign impurities) that result directly in carrier trapping. Finally, the polarity of the dielectric interface may also play a role, as it can affect local morphology or the distribution of electronic states in the OSC.

Inorganic Insulators and Surface Treatments

The first OFET devices frequently used Si substrates patterned by photolithography and SiO_2 as the insulator.[5] The choice of Si test devices was convenient, as SiO_2 can be thermally grown on the heavily doped Si wafers serving as the gate electrode. Although SiO_2 has been well-optimized to form a defect-free interface with Si, its top surface (relevant for an OFET) is much less defined, as it is subjected to ambient processing steps during OFET fabrication. The SiO_2 surface is likely to contain Si−OH defects and water, depending on its processing history. Alkali ions in the oxide layer influence further the quality of device characteristics, particularly hysteresis and threshold voltages. Surface states on inorganic oxides are a particular problem leading to interface trapping and hysteresis. Trapped charge is especially a problem with Si_3N_4. It is not surprising, therefore, that the use of SiO_2, Si_3N_4, and Al_2O_3 insulators in OFET research often still leads to low mobility and a high degree of variability.

The nature of the oxide interface also impacts the semiconductor morphology. Test devices involving inorganic oxides mostly employ the bottom gate architecture, and the dielectric−being also the substrate−influences morphology and device performance. The growth of pentacene on SiO_2 has been widely studied under different deposition conditions.[2,6,7] Importantly, it was demonstrated that the nucleation density was strongly influenced by the substrate quality: grain sizes were larger on Si(001) surfaces passivated with a cyclohexene layer than on SiO_2.[8] Dendridic growth in pentacene is often associated with high mobility and is typically achieved when the substrate temperature is between 20 and 130 °C, with a deposition rate of 1−3 Å/s.[7]

How much the dielectric substrate matters is clearly demonstrated by the large number of surface treatment studies in the literature. Surface treatments such as hexamethyldisilazene (HMDS) were first employed at Philips in the early 1990s to protect SiO_2 and define a uniform layer on top of it before depositing the OSC. HMDS is used in standard silicon processes to prepare surfaces before applying photoresists.[9] Several studies since investigated the effect of self-assembled monolayers (SAMS), such as HMDS,[10,11] octadecyltrichlorosilane (OTS),[12−18] other silanes,[14,17] alkanephosphonic acid,[19,20] or cinnamic[21] agents, which covalently attach to the SiO_2 or alumina dielectric. Mobility increase has been characteristic for many organic semiconductors. A possible explanation for increased field effect mobility is the increased grain size of the semiconductor. This, in turn, is assisted by high molecular surface mobility and reduced interaction with the surface of the hydrophobic substrate. Surface energy is greatly reduced on silanized substrates, and very high contact angles (>100°) with water are obtained. Increased grain size associated with SAMs was reported for pentacene.[12,14,15,22] A 2−10-fold mobility increase and reduced subthreshold slope was reported in pentacene, naphthalene, sexithiophene, and copper phthalocyanine OFETs when OTS or other silane treatment was applied on the SiO_2 dielectric.[15] In the case of pentacene, mobilities as large as 2.1 $cm^2\ V^{-1}\ s^{-1}$ were obtained. Increased grain size could indeed be demonstrated by AFM on pentacene and naphthalene thin films. There are, however, examples when very large contact angles (115°) on fluorinated alkanes resulted in small grain size.[14] In other studies it was reported that the use of OTS actually reduces pentacene grain size.[16,23] One suggestion, indicated by scanning electron microscopy (SEM) and X-ray diffraction (XRD), is that OTS may increase the density of flat-lying molecules and is responsible for increasing the hole mobility.[16] Longer alkyl and branched alkyl chains have been particularly effective, increasing the mobility up to 3.3 $cm^2\ V^{-1}\ s^{-1}$ and, although hydrophobic, reported to lead to a high degree of continuity in the first few molecular layers.[20] The long alkyl chains may also improve the smoothness of the dielectric layer.

Very high surface mobility can sometimes be counterproductive, as it leads to island growth with voids between and increased variability of device performance

across a substrte.[22] Interestingly, when studying a range of silane treatments, the IBM group found that the hydrophobicity alone could not explain the observed differences in pentacene performance.[14] The orientation of the terminal groups on the SAM appeared to be crucial; terminal bonds parallel to the surface produced highly ordered films with increased grain size and carrier mobility.

The most commonly accepted optimal orientation for pentacene is the long axis of the molecule being perpendicular to the substrate. Dielectric surface treatments for oligomers and polymers could also lead to favorable orientation.[10,11,13,17] In the highest mobility P3HT devices, lamella-like structure with the alkyl pendant chains perpendicular to the substrate was revealed by XRD.[11] This type of morphology has been promoted by the use of HMDS. In polyfluorene (F8T2) OFETs employing trichlorosilane surface layers, mobility also increased;[17] however, no sign of long-range order could be associated with the increase. OTS and benzyltrichlorosilane (BTS) resulted in mobilities of 1.5×10^{-2} and 5×10^{-3} $cm^2\ V^{-1}\ s^{-1}$ respectively, compared to 7×10^{-3} $cm^2\ V^{-1}\ s^{-1}$ on untreated SiO_2. Wetting properties of a number of different trichlorosilane SAMs did not correlate with the mobility. Instead, it was concluded that induced dipole interactions between similar features on the OSC and the dielectric surface may be operative but without inducing any order. Interestingly, SAM layers with built-in dipoles (e.g., a fluorosilane) could be shown to modify the threshold voltage dramatically.

In addition to morphology effects, SAMs can prime the dielectric to provide a more uniform interface. One of the most effective treatments, OTS, introduced by the Jackson group, is not only bonded to the substrate but also cross-linked laterally. OTS is not a monolayer, and due to the high density of interchain cross-linking, it may also reduce the surface roughness.[24] Surfaces exhibiting roughness greater than 3−5 Å have been reported to reduce the mobility in pentacene films.[23,25,26]

A recent, yet unpublished study at Philips investigated the link between the water contact angle of SiO_2 dielectric surface treatments and mobility in P3HT transistors. A variety of silane primers were used, e.g., HMDS, OTS, and *N*-octadecyldimethyl[3-trimethoxysilylpropyl]ammonium chloride (DMOAP). Interestingly, there was a clear increase of mobility with increasing contact angle (Figure 2), with the mobility changing over 3 orders of magnitude. Analysis of the temperature dependence of the mobility suggested that the overlap factor between hopping sites was increased, which in turn means that the layer was more ordered. However, XRD studies did not reveal any significant increase in layer structuring. Note that in a parallel study the use of iodine as a dopant led to dramatic changes in crystallinity detected by XRD, yet the mobility remained unchanged. (Iodine, being an electron acceptor, is an effective dopant and was primarily expected to affect the mobility via changing the free carrier concentration).

Contact angles were also investigated at Avecia on HMDS-treated SiO_2. Generally, there are two reported methods of applying HMDS. The first method involves baking the silicon wafers in an oven and subsequently introducing a vapor of the HMDS, which self-assembles

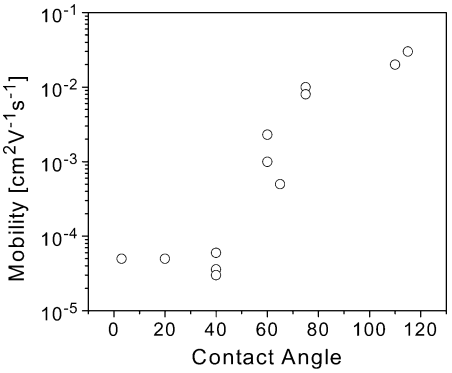

Figure 2. Field effect mobility in bottom gate P3HT devices as a function of water contact angle on the gate insulator. The insulator was SiO_2 with a variety of surface treatments affecting the surface energy (previously unpublished data from Philips).

onto the surface.[9] The second is a wet chemistry approach that involves boiling the substrates in a solution of the HMDS molecules.[10] The wet chemistry approach was found to be difficult to reproduce reliably, with mobility values varying by over an order of magnitude from one process to another. Static water contact angles have not been useful as a method of determining the quality of the surface treatment, since two substrates with an almost identical surface energy (~90° static angle to water and apparently high degree of silane coverage) have resulted in transistors with mobilities of $<10^{-4}$ to 2×10^{-3} $cm^2\ V^{-1}\ s^{-1}$ for the same triarylamine semiconductor material. Low contact angles, however, almost always led to low mobility for polymers such as PTAA, P3HT, and F8T2. It is possible that due to the hygroscopic nature of the HMDS molecules, the surface treatment is very sensitive to the level of water in the solvents and reaction vessels. Significant variability was also observed depending on the type of SiO_2 used, and it was concluded that the treatment was very difficult to make reproducible enough for reliable OFET experiments.

It can be seen that the interpretation of surface treatment effects on inorganics is often contradictory in the literature. The role of the dielectric surface treatments is still not entirely clear and may be a combination of several effects such as influencing surface energy and smoothness, inducing molecular orientation, and neutralizing surface defects. It is very interesting that some of the surface treatments discussed above improve OFET performance even when the semiconductor is amorphous.[27]

Organic Insulators

The dielectric systems discussed up to now have all been part of bottom gate devices. The deposition of inorganic dielectrics would be difficult on top of the OSC. The surface treatments employed on inorganics would be practically impossible to use in top gate devices. Organic dielectrics, however, offer the freedom to build both top and bottom gate devices more easily by the use of solution coating techniques and printing. Some organic insulator materials reported in the literature are shown in Figure 3.

Pentacene growth was compared on organic and inorganic dielectrics such as SiO_2, Si_3N_4, PVP, and

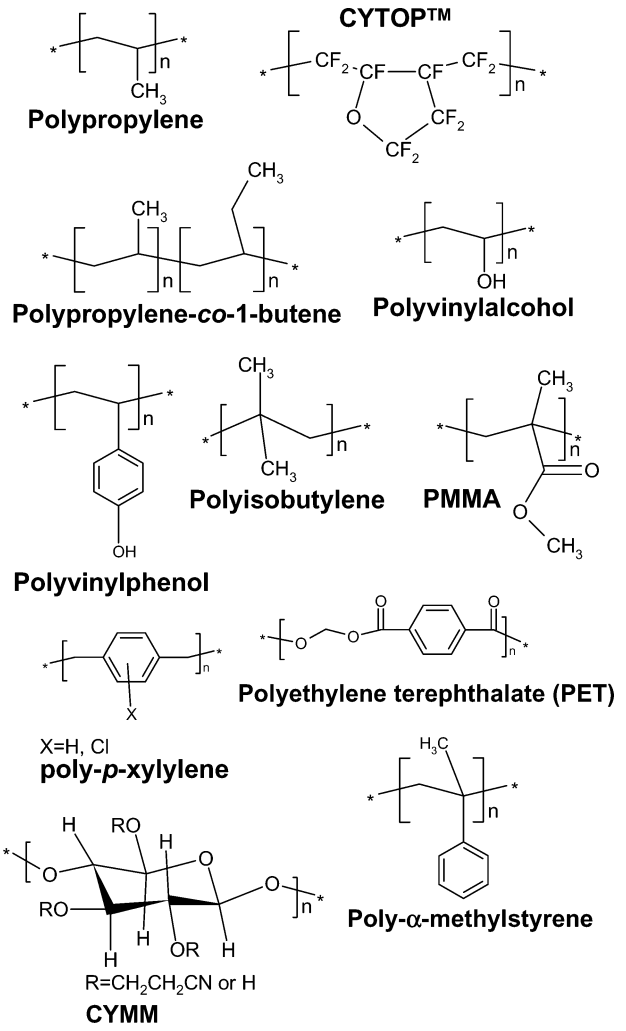

Figure 3. Organic polymers used as gate insulators.

benzocyclobutene (BCB),[26] all in bottom gate systems. Some difference in crystal sizes was observed, but it did not lead to significant differences in mobility or subthreshold swing. It was suggested that once deposition conditions are optimized for similar morphology, the intrinsic behavior of the pentacene controls device operation. The surface roughness, however, appeared to be a very important parameter, and polymeric insulators can generally produce smooth surfaces. The interface roughness between poly(9,9-dioctylfluorene) (PFO) and deuterated PMMA dielectric has been studied by neutron reflectivity, was found to be on the order of 10−20 Å, and was shown to be controlled by the final annealing temperature while insensitive to the processing history itself.[28]

In a very interesting study, the 3M team used thin, 10 nm layers of poly(a-methylstryrene) (αMS) on top of the SiO_2 dielectric.[29] Pentacene, deposited on the αMS layer yielded mobilities up to 5 $cm^2\ V^{-1}\ s^{-1}$, independent of the molecular weight of the styrene polymer. The presence of the αMS layer was the strongest contributor to high mobility among the other parameters studied, such as chamber pressure, deposition rate, and the number of crystal grains. It was also found that crystal size or the type/shape of grains was difficult to correlate with mobility.

The use of organic polymers such as PMMA has generally resulted in higher mobilities and better device

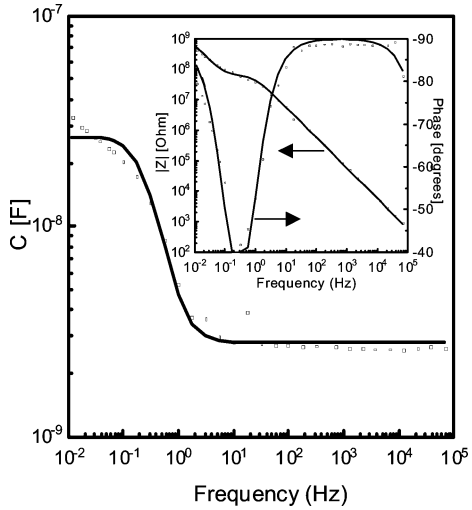

Figure 4. Capacitance vs frequency for a CYMM metal−insulator−metal sandwich structure. The inset shows impedance and the very large change of phase shift at low frequencies. Such insulators result in a considerable level of hysteresis.

reliability compared to the highly process dependent SiO_2. For example, mobilities in bottom gate α,ω-dihexylsexithiophene (DH6T) devices have been higher with organic insulators such as Parylene-C, a polyimide; PMMA; and PET compared to that on untreated SiO_2.[30,31,32] A high permittivity resin, cyanopulluane (CYMM), was also compared to SiO_2 in conjunction with sexithiophene in bottom gate configurations.[32] The mobility with SiO_2 and PMMA was 2×10^{-3} and 4×10^{-3} $cm^2\ V^{-1}\ s^{-1}$, respectively. A mobility of 0.1 was reported with CYMM, however, hysteresis in this device might have increased the figure artificially. Figure 4 illustrates results from Avecia on the frequency dependence of the capacitance in CYMM layers. Note the very large increase of capacitance at low frequencies. This may be due to slow polarization effects or ionic impurities, both leading to artificially large currents when scanning even at moderate speed with parameter analyzers. OFET devices using such materials exhibit strong hysteresis.[33] A good gate insulator should preferably have no dependence of capacitance on frequency.

Interestingly, mobilities as high as 0.1−0.5 $cm^2\ V^{-1}\ s^{-1}$ were obtained using a relatively polar insulator, PVP in oligothiophene FETs.[34] The dodecyl substituted oligomers were vacuum evaporated onto the dielectric and were clearly well ordered for such a high mobility. The presence of long alkyl chains may provide some screening effect from dipolar effects as well as from interface defects on the insulator.

Philips successfully used commercial photoresists (e.g. SC100 from Olin Hunt) as dielectrics in bottom gate devices and reported mobilities of 10^{-2}, 3×10^{-3}, and 10^{-3} $cm^2\ V^{-1}\ s^{-1}$ for precursor pentacene, P3HT, and poly(thienylene vinylene) (PTV), respectively.[35] P3HT is one of the materials studied most extensively in several research groups. Table 1 shows representative mobilities reported with different (both organic and inorganic) dielectrics over the past few years. Data that relates to P3HT polymers having a low degree of regioregularity or low molecular weight have been omitted here. The results are arranged chronologically with overlapping points adjusted on the *x*-axis for clarity. Mobilities range over 3 orders of magnitude in

Table 1. Field Effect Mobilities Reported in Regioregular P3HT with Different Dielectrics[a]

ref	year	dielectric	dielectric constant	surface treatment	structure	notes	mobility ($cm^2\ V^{-1}\ s^{-1}$)
36	1996	SiO_2	3.9	–	BG, BC	various solvents	$(1.5–4.5) \times 10^{-2}$
37	1997	polyimide			BG	dielectric and contacts screen-printed	3×10^{-2}
10	1998	SiO_2	3.9	HMDS	BG, TC		1×10^{-1}
11	1999	SiO_2	3.9	HMDS	BG	stacked alignment	$5 \times 10^{-2}–1 \times 10^{-1}$
35	2000	photoresist			TG, BC and BG, BC		3×10^{-3}
38	2001	PVP	4.5[b]		TG		2×10^{-1}
39	2001	SiO_2	3.9	HMDS	BG	doped P3HT	2×10^{-1}
40	2002	PVP	4.5		BG		5×10^{-2}
41	2002	copolymer blend	2.5		TG		2×10^{-2}
42	2002	(polyimide) SiO_2		HMDS	BG	reduced surface roughness	2×10^{-2}
43	2002	SiO_2	3.9	HMDS	BG	ultrathin P3HT layers	1×10^{-4}
44	2002	SiO_2	3.9	HMDS	BG		8×10^{-4}
45	2003	Al_2O_3	10	HMDS	BG		4×10^{-4}
46	2003	PVP	4.5		TG	vertical channel	1×10^{-2}
47	2003	SiO_2	3.9	HMDS	BG	various P3HT deposition techniques	2×10^{-1}
48	2003	PMMA	3.5		TG		5×10^{-2}
49	2003	SiO_2	3.9	OTS	BG		3×10^{-2}
50	2003	SiO_2	3.9	–	BG	μ dependence on charge	6×10^{-4}
51	2003	SiO_2	3.9	HMDS	BG		7×10^{-3}
52	2003	SiO_2	3.9	HMDS	BG		7×10^{-4}
this paper	2003	CYTOP	2.1		TG		2×10^{-2}
		PMMA	3.5		TG		7×10^{-3}
53	2004	TiO_2	41	HMDS	BG		5×10^{-3}
		(TiO_2) SiO_2	(41), 3.9	HMDS	BG		5.4×10^{-2}
		Al_2O_3	8.4	HMDS	BG		6.3×10^{-3}
		(Al_2O_3) SiO_2	(8.4), 3.9	HMDS	BG		8.5×10^{-2}

[a] BG = bottom gate device, TG = top gate device, BC = bottom contact device, TC = top contact device. For two-layer dielectrics, the layer not in contact with the semiconductor is in parentheses. [b] Note that reported dielectric constants for PVP vary in the literature. Here for consistency the number of 4.5 is used in agreement with Philips experience

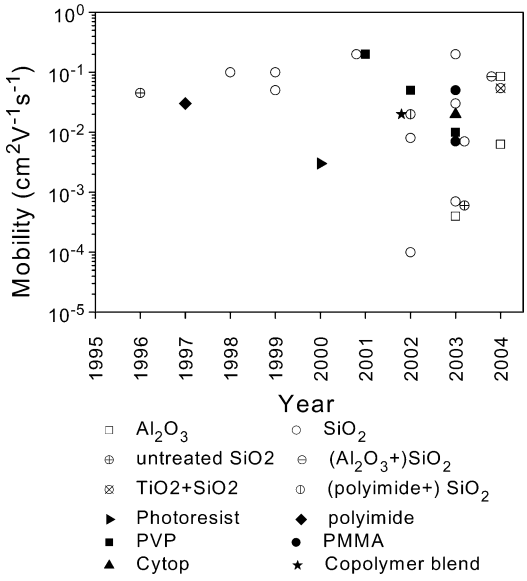

Figure 5. Mobilities in P3HT devices reported in the literature with different gate dielectrics. All open symbols relate to inorganic insulators, whereas closed symbols are for organic layers. If a second insulator layer is present but not in direct contact with the semiconductor, it is shown in parentheses.

different experiments; this variation is also well-illustrated in Figure 5. It is difficult to see correlations between the type of dielectric used and the carrier mobility, but clearly these results are highly influenced by the source of the polymer, deposition conditions, and the sensitivity of P3HT to ambient doping. Note that almost all workers reported the use of some surface treatment on inorganics. The highest variation is observed on inorganic dielectrics, which may be partly due to the type or quality of surface treatments.

The field effect mobility in P3HT is strongly gate voltage dependent, which can be another source for the variability of results. Figure 6 illustrates two top gate devices fabricated at Avecia, one with PMMA as the dielectric and the other with CYTOP. The use of these polymers as gate dielectrics has been discussed before elsewhere.[54] Note that the mobility is increasing as the gate voltage is raised and only at high gate voltages can one achieve mobilities approaching 0.01 $cm^2\ V^{-1}\ s^{-1}$. The mobility was calculated from the derivative of the drain current in the linear regime according to eq 1

$$\mu = \frac{\partial I_{DS}}{\partial V_G} \frac{L}{WC_i V_{DS}} \qquad (1)$$

where μ is the field effect mobility, W is the channel width, L is the channel length, and C_i is the gate capacitance. Although the calculation for μ is shown for the entire gate voltage range for all graphs in this paper, note that its validity is restricted to the linear regime i.e., when $|V_G| > |V_{DS}|$. The interesting point about these two P3HT devices is that both were prepared on the same PEN substrate, without any alignment process, and the dielectric deposition in this top gate configuration is not likely to change the morphology, yet the low polarity CYTOP fluoropolymer offers significantly better performance. Note that these P3HT devices were measured in a vacuum, otherwise on/off ratios would have been only about 10.

Nonpolar (low-k) organic insulators have been reported by Avecia to perform consistently better in *both* top and bottom gate devices.[33,54] Materials such as amorphous polytriarylamines (PTAA), fluorene–thiophene copolymers, P3HT, polyphenylene–vinylenes (PPVs), and even molecularly doped polymers showed

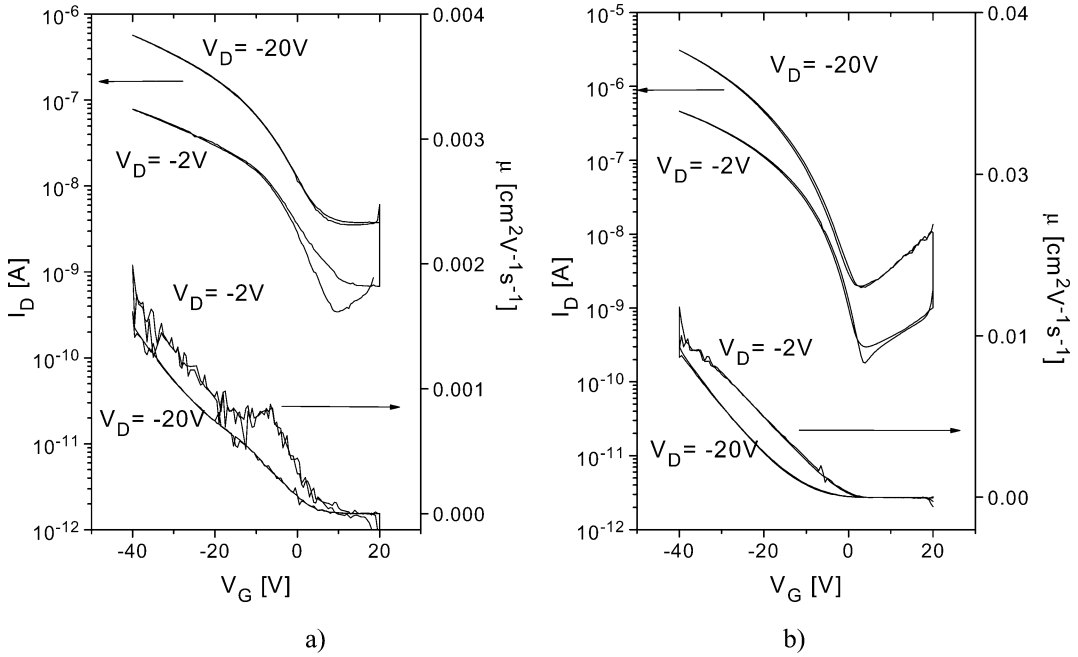

Figure 6. Transfer curves of top gate P3HT devices with (a) PMMA and (b) CYTOP as the dielectric. The gate capacitance in both devices is around 2 nF/cm^2. The mobility is also plotted against gate voltage on the right-hand axis. Note that the mobility curves are only correct and representative when V_G is greater than V_D. The measurements were performed in a vacuum; hence, reasonably high on/off ratio was achieved.

Table 2. Field Effect Mobilities Reported in F8T2 with Different Dielectrics[a]

ref	year	dielectric	dielectric constant	surface treatment	structure/ fabrication	mobility (cm^2/V s)
56	2000	PVP	4.5	rubbed polyamide substrate	TG, ink-jet printed	$(1-2) \times 10^{-2}$
59	2002	SiO_2	3.9	OTS	BG	4×10^{-4}
17	2002	SiO_2	3.9	various trichlorosilanes	BG	$7 \times 10^{-4}-1.5 \times 10^{-2}$
60	2002	copolymer blend	2.5		TG	1.5×10^{-2}
46	2003	PVP	4.5		TG, vertical channel	$(2-3) \times 10^{-3}$
54	2003	CYTOP	2.1		TG	1.5×10^{-3}
		PMMA	3.5		TG	3.3×10^{-4}
61	2003	polymer			TG, varying M_w	$(3-9) \times 10^{-3}$
62	2003	Si_3N_4	~7		BG, varying M_w	2×10^{-2}
63	2003	PVP	4.5		TG	1×10^{-3}
64	2003	(SiO_2) polyimide	(3.9)	polyimide rubbed to align chains	BG, thermally annealed	8×10^{-4}
65	2003	TiO_2	41		BG	4.7×10^{-5}
		Al_2O_3	8.4		BG	5.1×10^{-5}
		LPCVD Si_3N_4	7.4		BG	1.7×10^{-5}
		PECVD Si_3N_4	7.2		BG	1.6×10^{-5}
		SiO_2	3.9		BG	1×10^{-5}
66	2003	SiO_2	3.9	FDTS	BG	$(1-5) \times 10^{-3}$
57	2003	polymer			TG	$(4-6.9) \times 10^{-3}$
67	2003	SiO_2	3.9	OTS	BG	1×10^{-2}
68	2003	(BCB) Si_3N_4			BG	2.5×10^{-3}

[a] BG = bottom gate device, TG = top gate device, BC = bottom contact device, TC = top contact device. For two-layer dielectrics, the layer not in contact with the semiconductor is in parentheses.

increased mobility with low-polarity resins.[55] It was suggested that the mobility increased due to reduced dipolar (energetic) disorder at the interface, and the best results were obtained when the dielectric layer had a permittivity less than 2.2 and was homogeneous. The detailed mechanism will be discussed later in this review, in relation to amorphous OSC.

Table 2 summarizes some key results for another widely studied compound, F8T2, in combination with different dielectrics. These data is also shown in Figure 7, illustrating that despite the intensive device optimization work over the past years there is still significant scatter in the results. Again, it is noticeable that bottom gate inorganic dielectrics exhibit the highest degree of variation in mobility. Although F8T2 is a material that can be ordered, the mobility variation due to morphology in this polymer is probably much smaller than in P3HT. The highest mobilities for F8T2 (2×10^{-2} cm^2 V^{-1} s^{-1}) were obtained on rubbed polyimide substrates with PVP as the dielectric in top gate devices using a thermal anneal step to align the polymer chains through a liquid crystalline phase.[56] On a glass substrate, without rubbed alignment, optimized OFET devices of this polymer resulted in mobilties of 4×10^{-3} cm^2 V^{-1} s^{-1} in the amorphous state. This can be increased up to 7×10^{-3} cm^2 V^{-1} s^{-1} by increasing anneal temperatures.[57] The value for the amorphous polymer is in reasonable agreement with time-of-flight bulk mobilities in polyfluorenes.[58]

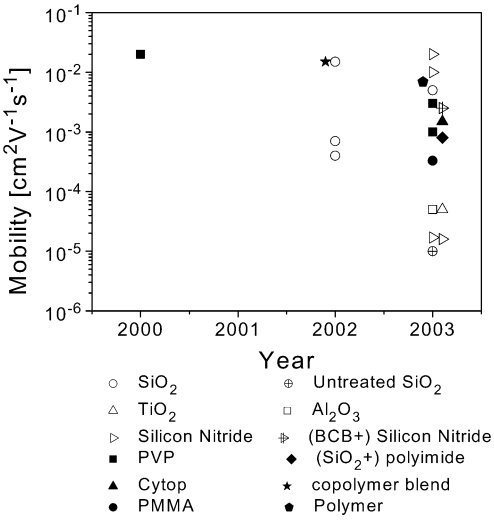

Figure 7. Mobilities in F8T2 devices reported in the past few years with different gate dielectrics. All open symbols relate to inorganic insulators, whereas closed symbols are for organic layers. If a second insulator layer is present but not in direct contact with the semiconductor, it is shown in parentheses.

The surface energy of organic gate insulators has been reported to affect mobilities when the insulator also acted as substrate in bottom gate devices. Yasuda et al.[69] studied a series of vapor-deposited poly-*p*-xylylene derivatives as insulators in bottom gate devices. The polymers studied had permittivities between 2.6 and 3.2. A good correlation was found between increasing mobility and high water contact angle on these dielectrics in the case of pentacene, copper phthalocyanine (CuPc), fluorinated CuPc (FCuPc), and even for amorphous poly[2-methoxy-5-(2′-ethylhexyloxy)-*p*-phenylenevinylene] (MEH−PPV). The mobility was most affected in MEH−PPV, and findings relating to this polymer were difficult to understand due to its amorphous nature.

Amorphous Semiconductors

Many of the leading materials currently used in OFET research have high intrinsic mobilities when the molecules are aligned in a particular orientation. Examples of such are pentacene, oligothiophenes, and P3HT. As discussed above, dielectric variations with these materials have often resulted in changes in mobility, and the explanation for the differences has focused upon the semiconductor morphology on the individual dielectric. While this may be true in many cases, there are some anomalous results suggesting that the semiconductor morphology may not be the only parameter influenced by changing the type of dielectric used in an OFET.[17,29,70] It is therefore useful to study the influence of the dielectric upon device performance in the top gate configuration, where the deposition of the semiconductor occurs prior to the dielectric deposition. Alternatively, one can use amorphous semiconducting materials that do not show any dependence of the mobility upon orientation. Unfortunately, there are few examples in the literature of top gate transistors made using highly oriented semiconductors. However, amorphous semiconductors are ideal to make OFETs with a variety of dielectrics in both top and bottom gate configurations and isolate effects relating to morphology.

Table 3. Field Effect Mobilities Achieved with Different Gate Insulators and Triarylamine Semiconductor Polymers

gate insulator	insulator permittivity	OSC	device type	μFET ($cm^2\ V^{-1}\ s^{-1}$)
CYTOP	2.1	PTAA2	top gate	5×10^{-3}
CYTOP	2.1	PTAA1	top gate	2×10^{-3}
polypropylene-*co*-butene	2.3	PTAA1	top gate	2.56×10^{-3}
polypropylene-*co*-butene	2.3	PTAA1	bottom gate	2.0×10^{-3}
PVP	4.5	PTAA1	top gate	5.2×10^{-4}
PMMA	3.5	PTAA1	top gate	4.9×10^{-4}
PMMA	3.5	PTAA2	top gate	5.5×10^{-4}
PVP-*co*-PMMA	~3.5−4	PTAA1	top gate	4.6×10^{-4}
polypropylene	2.1	PTAA1	top gate	1.7×10^{-3}
polyisobutylene	2.2	PTAA2	top gate	5×10^{-3}
polyisobutylene	2.2	PTAA2	bottom gate	5×10^{-3}
poly(vinyl alcohol)	10.4	PTAA1	top gate	8×10^{-5}
CYMM	18	PTAA1	top gate	$\sim 10^{-4}$ [a]
SiO_2	3.9	PTAA1	bottom gate	10^{-4}−10^{-5}

[a] The CYMM device resulted in highly gate voltage dependent mobility.

These also allow the investigation of critical parameters determining the suitability of a dielectric for plastic electronics applications.

Polytriarylamines (PTAA, Figure 1) are a range of highly stable semiconductors that are particularly useful to study dielectric effects in OFETs.[27,33,54] These polymers can be handled in air, and OFET devices are stable, operating at ambient conditions with mobilities above 10^{-3} $cm^2\ V^{-1}\ s^{-1}$. Their characterization is easier because morphology effects can largely be neglected. It also becomes possible to study carrier mobilities by independent means, such as time-of-flight (TOF). This makes them ideal candidates for studying electrical transport in OFETs. Mobilities measured by TOF are a very accurate representation of the bulk transport at low carrier concentrations. Some triarylamine polymers have consistently yielded bulk mobilities in excess of 10^{-2} $cm^2\ V^{-1}\ s^{-1}$ by TOF experiments.[27] However, field effect mobilities on dielectrics such as SiO_2 have been an order of magnitude lower.

The influence of a gate insulator on OFET mobility has been investigated using a number of different dielectric materials with amorphous polytriarylamines. Table 3 illustrates results for various device configurations.

The main finding of this work was that low polarity (low-k) resins resulted in far superior devices than PMMA or PVP. The latter polymers having permittivities around $\epsilon = 3.5$−4.5 resulted in approximately 10-fold mobility reduction compared to those with a permittivity of 2.1−2.3. Figure 8 illustrates differences in transfer curves with PMMA and a low-k resin. Mobilities are also plotted, using the same calculation discussed earlier for P3HT. Although conventional trends prefer high permittivity dielectrics, in this case the mobility increase more than compensates for the decrease in capacitance for comparable dielectric layer thickness. For PMMA ($\epsilon = 3.8$) in Figure 8a, the current flowing at $V_D = -20$V, $V_G = -40$V for a capacitance of 1.2 nF cm^{-2} is 0.122 μA. For the low-k dielectric ($\epsilon = 2.2$) (Figure 8b), at the same voltages and a capacitance of 2.0 nF cm^{-2}, the current flowing is 2.95 μA. Subthreshold slopes are also greatly improved with the low permittivity dielectric, to $S = 2.6$ V/decade compared

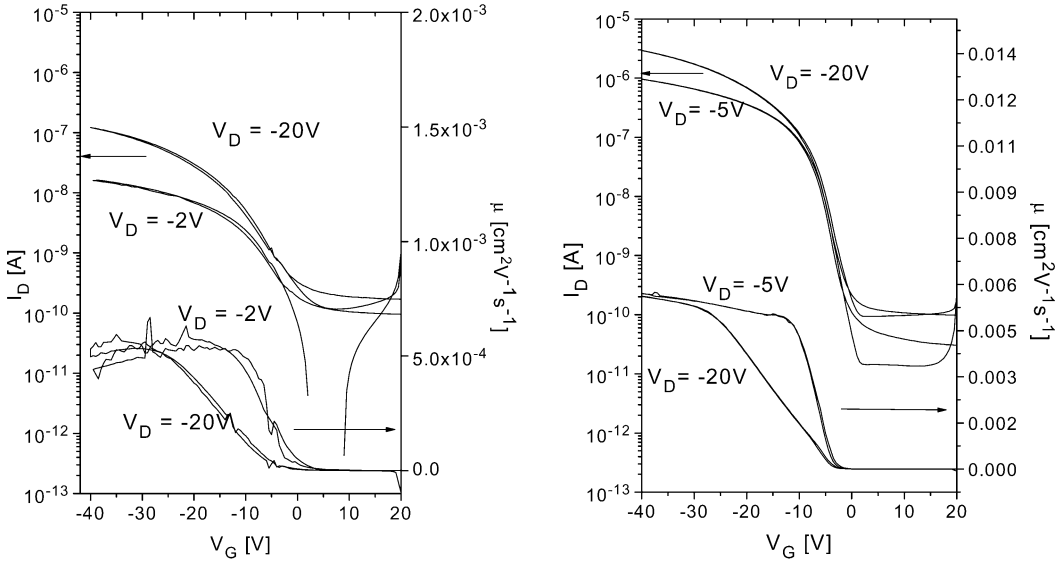

Figure 8. Transfer characteristics (I_D vs V_G) of top gate PTAA OFETs employing a dielectric of $\epsilon = 3.8$ (a) and a low-k dielectric of $\epsilon = 2.2$ (b). Device dimensions are $L = 100$ μm and $W = 36$ mm. The mobility is calculated in the linear regime (low V_D) and plotted continuously against gate voltage. Note that the mobility curves are only correct and representative when V_G is greater than V_D.

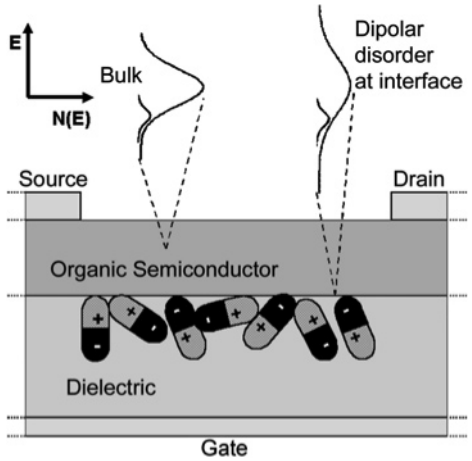

Figure 9. The density of states in the bulk of the semiconductor and at the interface with the dielectric. Local polarization may lead to an increase in the spread of site energies.

to $S = 8.5$ V/decade with PMMA. Using thinner dielectric coatings (<500 nm) values of S approaching 1 V/decade can be achieved. An additional benefit of the low-k dielectric is a reduced hysteresis between forward and reverse sweeps of the gate and in some cases improved threshold voltages.

Importantly, it was found that the temperature activation of the field-effect mobility increased when high permittivity insulators were used. This led to the hypothesis that localization is enhanced in the channel region if the interface is more polar and that randomly oriented interface dipoles modify site energies on the microscopic level. A common feature of organic semiconductors is that almost all sites can be considered localized and thus local variations in dipole orientation/chemistry have an influence on these sites, potentially scattering them in energy. Figure 9 illustrates how the bulk density of states is broadened according to this mechanism by dipolar disorder at the interface with the dielectric.

When the dielectric was of low polarity, the mobility achieved was very similar to the bulk mobility measured by TOF, and transport parameters extracted from the temperature dependence were also comparable. Improvements in the mobility due to low-k insulators were also seen with F8T2,[54] P3HT (see Figure 6), PPVs, and molecularly doped polymers.[55] Indeed, the key to obtaining good correlation between bulk and OFET mobilities was the use of an optimal, low polarity interface.[55] Some of the effective low-k gate insulators include copolymers of propylene, ethylene, isobutylene, and fluoropolymers. Examples are poly(perfluoroethylene-*co*-butenyl vinyl ether) (CYTOP, Asahi Glass), polypropylene-*co*-butene (PPCB), amorphous atactic polypropylene (PP), and polyisobutylene (PIB) (Figure 3). It was suggested that although the insulator has an impact on an essentially interfacial effect, an insulator of low polarity throughout its bulk might be more efficient than surface treatments. Note that residual reactive end groups are almost always present after surface treatments. Low-k insulators can provide a uniformly nonpolar and defect-free interface with the semiconductor independent of the deposition conditions. Nonpolar insulators are also suitable for top gate architectures where surface treatments could not be applied. It was also argued that low-k insulator layers ultimately provide a longer screening distance from polar sites and defects than surface treatments. The lifetime and stability of a homogeneous low-k dielectric is also likely to be better.

The strongest effect could be demonstrated when the permittivity of the dielectric was below 2.2 and the material was uniform. Materials that are low-k due to their porosity but contain ester, hydroxy, or acrylate functionalities are not well-suited. It must be noted, however, that the permittivity is not the only parameter for the optimal material choice, as the dielectric is also required to have high dielectric breakdown, yield a uniform and defect- and pinhole-free film, and be

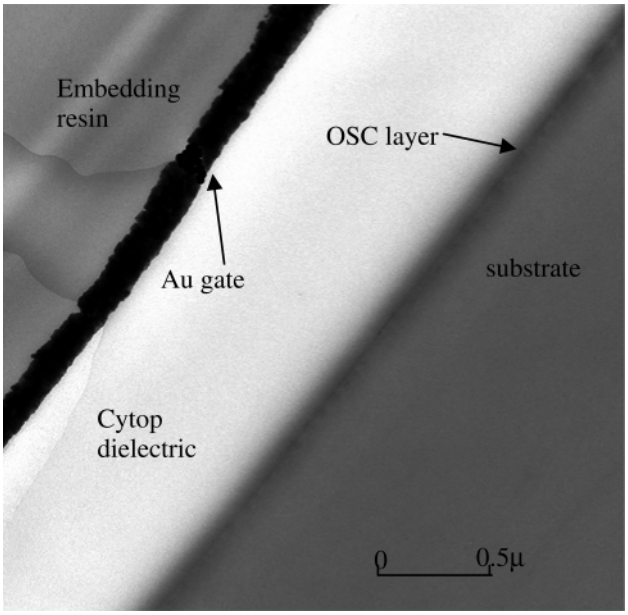

Figure 10. TEM image of cross-sectioned OSC device using low-k dielectric.

deposited from an orthogonal solvent to the semiconductor. Analysis of the morphology of the composite of layers is therefore important for overall device performance, and this can be achieved using several methods such as TEM (Figure 10), AFM, and neutron reflectivity.[28]

Using low-polarity insulators has enabled the development of materials with quite exceptional properties for amorphous systems in reliable test configurations. More recently, optimization of polymers through varying pendant substitution, molecular weight, polydispersity, and end-capping has resulted in devices exhibiting mobilities of 10^{-2} cm^2 V^{-1} s^{-1} in an OFET (see Figure 11).[71] The solution coatability of the semiconductor and dielectric make these materials well-suited for use in large area electronics manufactured by roll-to-roll techniques.

Very recently Philips also studied the performance of amorphous PTAA materials with different dielectrics. Bottom gate OFET devices were investigated using dielectrics with varying surface energies. On one hand, SiO_2 was used with different surface treatments, resulting in a range of water contact angles on the surface of the gate dielectric. On the other hand, polymeric photoresists were also tested, each having slightly different surface properties. It was found that the mobility monotonically increased as the dielectric surface became more hydrophobic (Figure 12). The highest mobilities obtained on high-quality OTS-treated SiO_2 (with a contact angle of 100°) resulted in mobilities close to 10^{-2} cm^2 V^{-1} s^{-1}, which is the bulk mobility of the PTAA polymer. Although a direct link between the permittivity of the organic photoresists was not seen (note that the range of organic resins investigated was limited), the results show that low surface polarity was beneficial to mobility.

It is not yet known whether the polarity of the OSC dielectric interface is a critical parameter for highly ordered materials beyond affecting their morphologies. Indeed, there are some examples of devices exhibiting high mobilities on both high- and low-k dielectrics. There is therefore the need to compare performance of OFETs made using these types of materials with high-k, low-k variations independently of morphology in both top and bottom gate devices.

Effects Related to the Gate Capacitance and Charge Density

High gate capacitance is a desirable parameter for FETs, because it allows a higher charge density to be induced at lower voltages and it increases drive capability. The capacitance can be increased by using a thinner dielectric or by using a high permittivity insulator material. Unfortunately, there is a limit to how thin the dielectric can be due to breakdown and reliability issues such as defects and yield. High permittivity inorganic materials such as barium titanate and barium strontium titanate were successfully used by the IBM group to reduce operating and threshold voltages.[72,73] Increased capacitance means that the semiconductor may operate in a different regime, with significantly higher

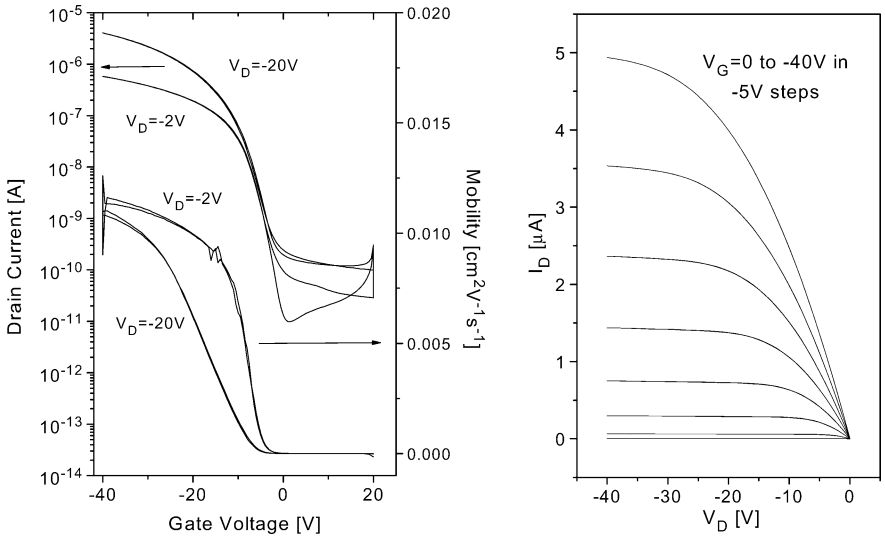

Figure 11. (a) Transfer curves for an OFET using optimized PTAA arylamine semiconductor (mobility = 0.01 cm^2 V^{-1} cm^{-1}, subthreshold slope 2.2 V/decade). (b) Output characteristics of the same device. Note that the mobility curves are only correct and representative when V_G is greater than V_D.

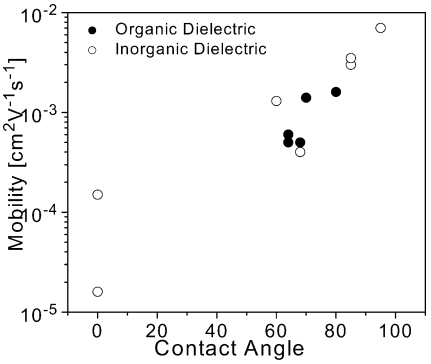

Figure 12. Field effect mobility in bottom gate PTAA devices as a function of water contact angle on the gate insulator. The insulator was either SiO_2 with a variety of surface treatments or commercial organic photoresists. (Previously unpublished data from Philips).

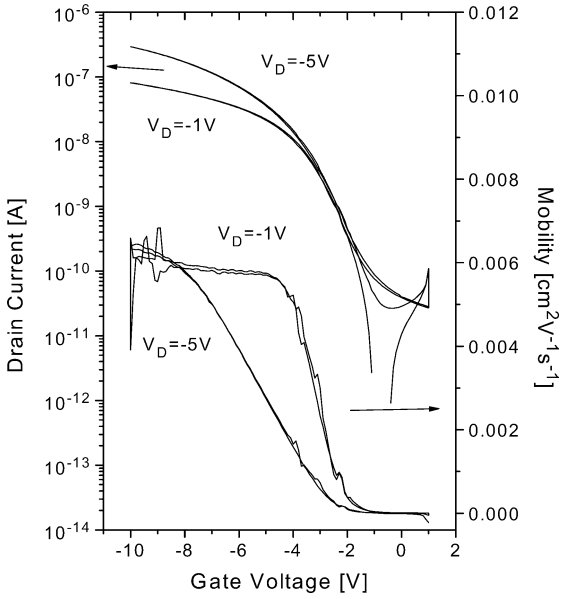

Figure 13. Transfer curve for a PTAA transistor operating at low voltages. The device is a top gate OFET employing a thin (400 nm) low-k (ϵ=2.2) dielectric. Note that the mobility curves are only correct and representative when V_G is greater than V_D.

density of carriers in the channel and/or reduced field acting perpendicular to the direction of transport. Increasing the gate capacitance enables trap states responsible for a threshold voltage to be filled at a much lower gate voltage, and further carrier accumulation will therefore result in free carrier flow.

Amorphous PTAA polymers may serve as model OFET systems to study such effects as they are relatively free of bulk or interface traps, domains, and grain boundaries.[27,33,54] In PTAA with optimal dielectric interfaces, the gate voltage dependence of the mobility is not significant and the device operation scales with the dielectric thickness. The mobility remains unaffected at high carrier densities in the channel, and this has been tested using gate voltages up to −200 V. Low voltage operation, without changing the mobility, is achieved by simply reducing dielectric thickness. Figure 13 shows a PTAA OFET fabricated with a thinner (400 nm) low-k dielectric. Early turn-on is observed at low voltages for a gate capacitance of 3.5 nF cm^{-2} with a threshold voltage of −1.5 V and a subthreshold slope around 1 V/decade. Neither the charge density nor the gate field appears to influence significantly the mobility. Such optimal operation is achieved by eliminating localized interface states through the use of low polarity interfaces. This can also lead to the reduction of threshold voltages without the need to induce more charge.[33]

This example of PTAA is unique and most OSC materials exhibit gate voltage dependence, which is often influenced by the dielectric interface. Several workers have reported a dependence of the mobility with accumulated charge for evaporated pentacene as the semiconductor. Dimitrakopoulos et al. demonstrated a strong rise in mobility of pentacene for various dielectrics as a function of accumulated charge. The mobility increased up to a value of 0.4 $cm^2\ V^{-1}\ s^{-1}$ for a charge concentration of 2 mC cm^{-2}, assuming that the accumulation region is two-dimensional and confined very close to the organic semiconductor−dielectric interface.[74] Further increase of the charge concentration resulted in a constant mobility value. A high-k dielectric BZT was used as the gate insulator.[2] The authors concluded that increasing the capacitance through the dielectric constant provided an efficient way of obtaining the highest possible mobility with the lowest driving voltage, at low gate fields. Völkel et al.[75] modeled the gate dependent mobility effect for pentacene by incorporating localized intraband states. They observed a larger voltage sweep before saturation of the mobility and hence deceptively lower mobility values for fixed gate voltages. The authors stated that the gate voltage induced charge into localized states as well as band states, thereby reducing the effective mobile charge concentration at the semiconductor−dielectric interface. This led to a gradual increase of the mobility with gate voltage.

F8T2 has been investigated by Swensen et al.[65] with various inorganic dielectrics to increase capacitance. The authors quoted mobility between 1×10^{-5} and 5×10^{-5} $cm^2\ V^{-1}\ s^{-1}$ for F8T2 devices without a "mobility-enhancing" monolayer at the semiconductor dielectric interface using the dielectrics TiO_2 and Al_2O_3, two different types of silicon nitride, and SiO_2. The structure used photolithographically patterned gold electrodes on top of the organic semiconductor, which was spin-cast on the dielectric. The authors noted comparable performance between the various dielectric devices when results were normalized for charge induced by the gate. Lower threshold voltages and steeper subthreshold slopes were observed in the higher capacitance devices (TiO_2 and Al_2O_3), allowing lower operating voltages. The slight variation in device performance led the authors to believe that interface traps, although present and filled faster for high capacitance devices, did not control the mobility of the material and that bulk traps had a dominant effect in the low mobility of the F8T2.

Operating voltage and threshold voltage have also been successfully reduced by high-k insulators used in polymeric FETs. Bartic et al.[76] used tantalum pentoxide (Ta_2O_5) evaporated by electron beam to fabricate both top-gate and bottom-gate devices with P3HT as the semiconductor. A dielectric constant of 21 enabled capacitance values up to 180 nF cm^{-2}, giving operating voltages as low as −3 V.

Chemically anodized aluminum oxide (alumina) has been used as a dielectric by the groups at Liverpool[45] and Sheffield University.[77] The Sheffield group also produced FETs on ~5 nm alumina films, giving capacitances in excess of 600 nF cm^{-2}.[78] In this case, operating voltages were reduced to about −2 V with threshold voltages of −0.7 V.

More recently, Wang et al.[53] used titanium dioxide (TiO_2, dielectric constant ~41) deposited by an RF physical vapor deposition system with a P3HT semiconductor (see Table 1). The authors were able to achieve capacitances in the range 147−750 nF cm^{-2} with operating voltages from around 0 to −5 V and threshold voltages less than 1 V. It was noted that pure TiO_2 was very leaky and required a silicon dioxide capping layer to passivate the surface. Leakage current in oxides is known to be dependent on the energy band of the dielectric, specifically energy gap and band offsets (the difference between conduction and valence bands in the oxide to the semiconductor).

Organic materials typically do not produce very high dielectric constants (ϵ). Some of the highest k organic materials are poly(vinyl alcohol) ($\epsilon \sim 10$) and cyanoresins (e.g. CYMM, $\epsilon \sim 18$). Parashkov et al.[79] have investigated both types of dielectric with a polythiophene derivative semiconductor. The authors reported mobility dependence on dielectric solvent and increasing mobility with the higher dielectric constant materials. Unfortunately, highly polar organic polymers are also likely to contain water and ionic impurities. The authors of this review found CYMM and PVA to modulate OFET currents reasonably well. However, after close investigation it was found that slow polarization effects (Figure 4), possibly due to mobile ions, were responsible for large hysteresis and led to the overestimate of the mobility.[33] Bao et al.[37] investigated relatively high capacitance devices (~20 nF cm^{-2}) using thin layers of screen-printed polyimide (ϵ~3) and regioregular P3HT as the semiconductor. The group reported mobilities of up 0.03 cm^2/V s, some of the highest reported for printed organic FETs.

Note that threshold voltages are difficult to define when the mobility is gate voltage dependent. P3HT is a good example (Figure 6a,b)−V_{th} is difficult to define if one attempts to draw an asymptote to $I_D(V_G)$ in the linear regime. The threshold voltage may also include contributions due to contact effects at the source and drain electrodes and due to trapped charge in the gate dielectric itself.[80]

The above works demonstrate that threshold voltages may be reduced effectively by increasing the gate capacitance. This is normally possible irrespective of whether V_{th} is due to built-in charge, contact effects, or interface trapping. Defect states in both the bulk of the OSC and at the dielectric interface can influence the threshold voltage and lead to shallow subthreshold operation. Strategies leading to the reduction of these states are highly desirable. At the same time the mechanism of how the induced charge density influences the mobility itself is still a controversial topic. Studies at Philips suggested that the mobility increases with charge density, but its dependence is dominated by the shape of the DOS. For systems with 3D transport and relatively low mobilities, typically a strong increase was observed, and this could be rationalized by the apparent mobility increase in OLEDs as the current density is increased at the space charge limited (SCLC) regime.[50,81] The above description was suggested to hold for a Gaussian DOS, while for highly ordered systems LED (i.e. bulk) and FET mobilities cannot be compared. Note that in some OFET devices the mobility actually decreases with increasing charge density, which is a puzzling phenomenon. One explanation may be the effect of increased gate field forcing carriers to move through less favorable interface states; however, the only way to distinguish between gate field and charge density is to vary the permittivity of the dielectric, which may influence other factors such as OSC morphology. Sancho-García et al.[82] calculated the effect of the gate field on the reorganizational energy of molecular orbitals and concluded that the gate field is expected to have little impact on transport properties. However, the rate-determining step in transport is likely to be slow states, i.e., "dead-ends" in a molecular network, where a high field can significantly reduce escape probability perpendicular to the direction of transport.

Summary

Organic field-effect transistors are interface devices, operating typically in enhancement mode. The region where charge transport takes place, the accumulation layer, has a thickness of only a few nanometers. It is therefore not surprising that both the semiconductor and the gate dielectric affect the operation of a device. Due to the relatively low mobilities in organic materials, the interface is especially critical and can have a strong impact on electrical transport itself. This is particularly evident from the large variation of mobilities reported for the same organic semiconductor material. The variation persists despite significant optimization of material deposition techniques, e.g., solution processing, spinning, drop casting, printing, and vapor deposition.

Numerous combinations of organic semiconductors and gate dielectrics have been reported in the literature. Inorganic compounds such as SiO_2, Si_3N_4, Al_2O_3, and a variety of organic polymers have been used. Surface treatments have been widely used, especially for inorganic insulators, in order to modify the interface. Reported mobilities exhibit perhaps the largest scatter on inorganic dielectrics, which may be due to inorganic surface states or the quality and type of the surface treatment. In bottom gate devices, the dielectric surface affects critically the semiconductor morphology, which itself is the single most important parameter for high mobility in materials exhibiting crystallinity or self-ordering. It is striking that almost all semiconductor materials perform better when deposited onto hydrophobic dielectric surfaces. Explanations for this range from enhanced surface mobility (and therefore enhanced crystallinity and increased domain size) to improvement in the relative orientation of molecular segments to the surface. However, observations relating domain size and nucleation density do not always agree, and the interpretation of surface treatment effects also varies considerably.

The interplay between insulators and OSC is complex, and a full interpretation of it is not yet available. However, some clear trends emerge that suggests that

there are a number of effects not solely related to OSC morphology. Clearly, the interface roughness should be as small as possible, and intermixing between OSC and dielectric layers should be negligible; otherwise, trap states are developed in the channel. This is particularly critical when solution deposition is used. The choice for solution-coated dielectrics has been mostly materials that are much more polar than the OSC (i.e. alcohol soluble), but more recently, nonpolar dielectrics were employed using nonpolar solvents. The latter have been shown to be remarkably effective for top gate OFETs, where the dielectric is unlikely to change the OSC morphology. Examples shown in this paper are for regioregular P3HT. Amorphous OSCs also appear to benefit from a low polarity interface both in top and bottom gate OFETs. A hypothesis relating surface polarity to enhanced localization was put forward to explain this intriguing effect. Although conventionally high permittivity dielectrics have been preferred to maximize capacitance, the mobility increase may be more than enough to compensate for reduced capacitance with low-k dielectrics. Low polarity interfaces also ensure that the amount of water present at the interface is minimal.

The measure of polarity may be the contact angle of water on the insulator surface or the dielectric constant itself. Both are "average" properties inasmuch as a good surface treatment with high degree of hydrophobicity does not necessarily mean full and continuous coverage. In the same way, a low bulk dielectric constant (ϵ) does not necessarily result in a nonpolar surface if the dielectric contains nonpolar segments alternated by polar ones (or low ϵ is achieved only by porosity). However, if most monomer units are nonpolar and the material is homogeneous, a high degree of uniformity can be achieved easily. The reliability of such layers may be much better than that of surface treatments. Being thicker (several 10 nm at least), they can also provide better screening from polar defect sites. Some surface treatments, such as OTS, may be more effective due to their thicker coverage through lateral cross-linking or long alkyl chains. The literature reports improved trends observed both against water contact angle and bulk polarity (dielectric constant) of the insulator.

The issue of polarity may also be viewed from a different angle. In general, it is desirable to maximize interactions between OSC molecular segments and minimize interactions between the OSC and the dielectric layer. Since the only interactions operating are of van der Waals type, this may be best achieved by minimizing chances for both hydrogen bonding and dipole forces between the dielectric and the OSC. Incidentally, this also leaves the greatest freedom for molecular mobility and alignment between OSC molecular segments, leading to a higher degree of crystallinity. In addition, this is likely to minimize chances for intermixing between the OSC and the dielectric. Unfortunately, wetting and adhesion may be reduced when coating from solution onto highly hydrophobic surfaces; therefore, a careful balance is required for a practical solution.

The dielectric interface is likely to be a critical factor for real applications in flexible electronics. Many more experiments will be required in order to understand more fully interface phenomena, especially those able to separate morphology effects from others. For example, comparison of top and bottom gate devices on the same substrate would be very interesting. Gate voltage dependent mobility and subthreshold operation are not well-understood yet. Both of these are likely to offer interesting insight into interface related phenomena.

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